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10/758,971	01/15/2004	Kenji Yamagami	16869B-080700US	6513

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EXAMINER	
YU, JAE UN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	10/758,971	YAMAGAMI, KENJI	
	Examiner	Art Unit	
	Jae U. Yu	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the applicant's submission of the amendment dated 9/17/2007. At this point claims 1, 10, 19, 22 and 23 have been amended and claim 2 has been cancelled. Thus, claims 1 and 3-23 are pending in the instant application.

Response to Amendment

In view of the applicant's amendment, the examiner directs the applicant's attention to the following new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3-5, 7-15, 18 and 23 are rejected under 35 U.S.C. 103 (a) as being obvious over Nakamura et al. (US 2002/0078296) in view of De Margerie et al. (US 6,859,865) and Fukuzumi (US 2002/0083263).

2. As per **independent claims 1 and 10**, **Nakamura et al. disclose,** "an intermediate storage subsystem **["Main Center" 101, Figure 1]** including a write-order-information provider **["MCU", Paragraph 80]** that is configured to generate write-order information **["Time Stamp & Sequence Number", Paragraph 80]** for the write data,

wherein the intermediate storage subsystem includes intermediate volumes **["Vols", Figure 1]** defined as a consistency group within which data integrity is guaranteed **[Mirroring System, Figure 1]**".

"First and second secondary storage subsystems coupled to the intermediate storage subsystem **["S-Vol" 111, Figure 1]** configured to receive the write data from the intermediate storage subsystem **["Main Center" 101, Figure 1]**, the first secondary storage subsystem including a first secondary volume **["S-Vol" 111-1, Figure 1]** that is configured to mirror the first primary volume, the second storage subsystem including a second secondary volume **["S-Vol" 111-2, Figure 1]** that is configured to mirror the second primary volume, wherein the write data are stored in the first and second storage subsystems according to the write order information **["Write data are rearranged in the sequence number within the RCU 104", Paragraph 80]** associated with the write data as generated by the write-order-information provider of the intermediate storage subsystem which is a separate storage subsystem from the first primary storage subsystem having the first primary volume and the second primary storage subsystem having the second primary volume" **Nakamura et al. disclose "S-Vol" 111-1 & 111-2 ("First & second secondary storage subsystem" from the claim) configured to mirror "P-Vol" asynchronously 108-1 & 108-2 in paragraph 34.**

Nakamura et al. do not disclose expressly, "first and second primary storage subsystems, the first primary storage subsystem including a first primary volume, the second primary storage subsystem including a second primary volume, the first and second primary volumes storing a plurality of write data in a given order".

De Margerie et al. disclose first and second primary storage 22a & 22b that are mirrored synchronously by first and second secondary storages 32a & 32b in Figure 1 and (Column 4, Line 54 – Column 5, Line 35).

Nakamura et al. and De Margerie et al. are analogous art because they are from the same field of endeavor of storage mirroring.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Nakamura et al. by including synchronously mirrored storages as taught by De Margerie et al. in Figure 1.

The motivation for doing so would have been to guarantee that data is securely stored even if either the primary or secondary storages are destroyed as expressly taught by De Margerie et al. in Column 1, Lines 43-45.

Therefore, it would have been obvious to combine De Margerie et al. with Nakamura et al. for the benefit of secure data backup to obtain the invention specified in claim 1.

De Margerie et al. and Nakamura et al. do not teach expressly that the intermediate storage subsystem is "not directly coupled to a host unit".

Fukuzumi discloses the "Buffer Memory" 4 coupled in between the host unit and the flash memory in Figure 1.

De Margerie et al., Fukuzumi and Nakamura et al. are analogous art because they are from the same filed of endeavor of controlling a plurality of storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify De Margerie et al. and Nakamura et al. by including a buffer between a host unit and a storage system as taught by Fukuzumi in figure 1.

The motivation for doing so would have been the cost efficient storage device as expressly taught by Fukuzumi in paragraphs 23 and 24.

Therefore, it would have been obvious to combine Fukuzumi with DeMargerie et al. and Nakamura et al. to obtain the invention as specified in claims 1 and 10.

3. **Claim 3** discloses, "the write-order-information provider is a counter that generates a sequence number **["Sequence Number", Paragraph 80]** to be attached to the write data received from the primary system".

4. **Claim 4** discloses, "the intermediate subsystem includes first and second intermediate volumes **["P-Vol" 108-1 & 108-2, Figure 1, Nakamura et al.]**, the first

intermediate volume being configured to receive the write data from the first primary volume **["Storage Device" 22a, Figure 1, De Margerie et al.]**, the second intermediate volume being configured to receive the write data from the second primary volume **["Storage Device" 22b, Figure 1, De Margerie et al.]**".

5. **Claim 5** discloses, "a valid counter provided in the intermediate subsystem, the valid counter being configured to keep the highest sequence number of the write data **["Time Stamp" configured to keep the highest sequence number (Seq#4 & Seq#5), Figure 3, Nakamura et al.]** that is ready to be validated for copying at the secondary subsystem".

6. **Claim 7** discloses, "the intermediate subsystem including a journal volume **["Memory" 116, Paragraph 30, Nakamura et al.]** to receive the write data from the first and second primary subsystems".

7. **Claim 8** discloses, "the first and second primary subsystems are disk array units **["Disk Storage Devices", Column 5, Lines 14-15, De Margerie et al.]**".

8. **Claim 9** discloses, "the primary subsystems are provided at a primary site **["Primary Site", Column 4, Lines 57-61, De Margerie et al.]** and the secondary subsystems are provided at a secondary site **["Remote Center" 103, Figure 1, Nakamura et al.]**".

"Wherein the secondary subsystems are configured to replace the primary subsystems as primary storage areas if either the primary subsystems or the primary host experiences failure or is taken off line **[Processing by utilizing data stored in the RCU 104, Paragraph 27, Nakamura et al.]**".

9. **Claim 11** discloses, "the first storage is configured to receive first and second write data from the at least one primary subsystem in a given order **[Paragraph 80, Nakamura et al.]**, the first and second write data being provided with first and second write order information **["Time Stamp & Sequence Number", Paragraph 80]**, respectively, by the intermediate subsystem".

"Wherein the first and second write data are stored in the at least one secondary subsystem **["S-Vol" 111, Figure 1, Nakamura et al.]** according to the given order using the first and second write order information **[Paragraph 80, Nakamura et al.]**"

10. **Claim 12** discloses, "the write-order-information provider is a counter configured to generate sequence numbers **["Sequence Number", Paragraph 80, Nakamura et al.]**, the generated sequence number being associated with the write data according to an order the write data are received from the at least one primary subsystem".

11. **Claim 13** discloses, "the first storage area is a journal volume **["Memory" 116, Paragraph 30, Nakamura et al.]** that is configured to receive write data from the plurality of primary subsystems".

12. **Claim 14** discloses, "a second storage area **["P-Vol" 108-2, Figure 1, Nakamura et al.]**".

"Wherein the plurality of primary subsystems including a first primary volume **["Storage Device" 22a, Figure 1, De Margerie et al.]** provided in a first primary subsystem, and a second primary volume **["Storage Volume" 22b, Figure 1, De Margerie et al.]** provided in a second primary subsystem"

"Wherein the first and second storage areas are first and second intermediate volumes, the first intermediate volume being configured to receive write data from the first primary volume and the second intermediate volume being configured to receive write data from the second primary volume" **De Margerie et al. disclose first and second primary storage 22a & 22b that are mirrored synchronously by first and second secondary storages 32a & 32b in Figure 1 and (Column 4, Line 54 – Column 5, Line 35).**

"Wherein the first intermediate volume is configured to send the write data received from the first primary volume to a first secondary volume **["S-Vol" 111-1, Figure 1, Nakamura et al.]** provided in a first secondary subsystem and the second intermediate

volume is configured to send the write data received from the second primary volume to a second secondary volume **["S-Vol" 111-2, Figure 1, Nakamura et al.]** provided in a second secondary subsystem"

13. **Claim 15** discloses, "a valid counter provided in the intermediate subsystem, the valid counter being configured to keep the highest sequence number of the write data **["Time Stamp" configured to keep the highest sequence number (Seq#4 & Seq#5), Figure 3, Nakamura et al.]** that is ready to be validated for copying at the secondary subsystems".

14. **Claim 18** discloses, "the intermediate storage subsystem is a disk array unit **["P-Vol", Figure 1, Nakamura et al.]**".

15. As per **independent claim 23**, the examiner interprets the claim according to 35 USC 112 Sixth Paragraph.

Nakamura et al. disclose, "means ("non-volatile storage area", paragraph 69 of the applicant's specification) **["Magnetic Disk Drive", Paragraph 30]** for receiving write data".

"Means ("sequence number", paragraph 44 of the applicant's specification) **["Sequence Number", Paragraph 80]** for generating write order information for the write data

["Write data are rearranged in the sequence number within the RCU 104", Paragraph 80], the write order information being associated with the write data, the write order information providing information as to a write order of the write data".

"Wherein the write order information is used to stored the write data in the first and second secondary volumes of first and second secondary subsystems **["Write data are rearranged in the sequence number within the RCU 104", Paragraph 80]** which are separate storage subsystem from the intermediate storage subsystem, the first secondary volume being **["S-Vol" 111-1, Figure 1]** defined in the first secondary subsystem, the second secondary volume **["S-Vol" 111-2, Figure 1]** being defined in the second secondary subsystem, wherein the intermediate storage subsystem asynchronously **[Paragraph 80]** transmits data to the first and second secondary subsystems"

"the intermediate storage subsystem including intermediate volumes **["Vols", Figure 1]** defined as a consistency group within which data integrity is guaranteed **[Mirroring System, Figure 1]**"

Nakamura et al. do not disclose expressly, "the first primary volume being defined in the first primary subsystem, the second primary volume being defined in the second primary subsystem, the write data being received synchronously from the

primary subsystems; wherein the first and second secondary volumes mirror the first and second primary volumes".

De Margerie et al. disclose first and second primary volumes 22a & 22b that are mirrored synchronously by first and second secondary storages 32a & 32b in Figure 1 and (Column 4, Line 54 – Column 5, Line 35).

Nakamura et al. and De Margerie et al. are analogous art because they are from the same field of endeavor of storage mirroring.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Nakamura et al. by including synchronously mirrored storages as taught by De Margerie et al. in Figure 1.

The motivation for doing so would have been to guarantee that data is securely stored even if either the primary or secondary storages are destroyed as expressly taught by De Margerie et al. in Column 1, Lines 43-45.

Therefore, it would have been obvious to combine De Margerie et al. with Nakamura et al. for the benefit of secure data backup to obtain the invention specified in claim 23.

De Margerie et al. and Nakamura et al. do not teach expressly that the intermediate storage subsystem is "not directly coupled to a host unit".

Fukuzumi discloses the "Buffer Memory" 4 coupled in between the host unit and the flash memory in Figure 1.

De Margerie et al., Fukuzumi and Nakamura et al. are analogous art because they are from the same filed of endeavor of controlling a plurality of storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify De Margerie et al. and Nakamura et al. by including a buffer between a host unit and a storage system as taught by Fukuzumi in figure 1.

The motivation for doing so would have been the cost efficient storage device as expressly taught by Fukuzumi in paragraphs 23 and 24.

Therefore, it would have been obvious to combine Fukuzumi with DeMargerie et al. and Nakamura et al. to obtain the invention as specified in claim 23.

16. Claims 19, 20 and 22 are rejected under 35 USC 103 (a) as being obvious over Nakamura et al. (US 2002/0078296) in view of De Margerie et al. (US 6,859,865), Fukuzumi (US 2002/0083263) and Peng (US 2002/0122601).

17. As per **independent claims 19 and 22**, Nakamura et al. disclose, "an intermediate storage subsystem **["Main Center", Figure 1]**".

"Associating first write order information to the first write data at the intermediate storage subsystem; transmitting asynchronously the first write data **[Paragraph 80]** and

the first write order information **["Time Stamp & Sequence Number", Paragraph 80]** to a first secondary storage subsystem **["S-Vol" 111-1&2, Figure 1, Paragraph 34]** which is a separate storage subsystem from the intermediate storage subsystem, the intermediate storage subsystem including intermediate volumes **["Vols", Figure 1]** defined as a consistency group within which data integrity is guaranteed **[Mirroring System, Figure 1]**".

"Associating second write order information to the second write data; transmitting asynchronously the second write data **[Paragraph 80]** and the second write order information **["Time Stamp & Sequence Number", Paragraph 80]** to a second secondary storage subsystem **["S-Vol" 111-3&4, Figure 1, Paragraph 34]** which is a separate storage subsystem from the intermediate storage subsytem, wherein the first and second write data are stored in the first and second secondary subsystems, respectively, according to the first and second write order information **["Write data are rearranged in the sequence number within the RCU 104", Paragraph 80]**"

Nakamura et al. do not disclose expressly, "receiving first write data from a first primary storage subsystem, the first write data being sent by the first primary subsystem synchronously; receiving second write data from a second primary storage subsystem, the second write data being sent by the second primary subsystem synchronously".

De Margerie et al. disclose first and second primary storage 22a & 22b that are mirrored synchronously by first and second secondary storages 32a & 32b in Figure 1 and (Column 4, Line 54 – Column 5, Line 35).

Nakamura et al. and De Margerie et al. do not disclose expressly that the above method is stored in "a computer readable medium" as a "computer program".

Peng discloses "software" in paragraph 9, which corresponds to the "computer program" from the claim. A "computer program" is inherently stored and executed in a computer system.

Nakamura et al., De Margerie et al. and Peng are analogous art because they are from the same field of endeavor of data management.
At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Nakamura et al. by including synchronously mirrored storages as taught by De Margerie et al. in Figure 1, and represent the remote copy operation as a computer program as taught by Peng in Paragraph 9.

The motivation for doing so would have been to guarantee that data is securely stored even if either the primary or secondary storages are destroyed as expressly taught by De Margerie et al. in Column 1, Lines 43-45, and "cost/flexibility advantages over hardware" as expressly taught by Pen in paragraph 9.

Therefore, it would have been obvious to combine De Margerie et al. with Nakamura et al. and Peng for the benefit of secure data backup and cost/flexibility to obtain the invention specified in claim 19 and 22.

De Margerie et al., Peng and Nakamura et al. do not teach expressly that the intermediate storage subsystem is "not directly coupled to a host unit".

Fukuzumi discloses the "Buffer Memory" 4 coupled in between the host unit and the flash memory in Figure 1.

De Margerie et al., Peng, Fukuzumi and Nakamura et al. are analogous art because they are from the same filed of endeavor of controlling a plurality of storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify De Margerie et al., Peng and Nakamura et al. by including a buffer between a host unit and a storage system as taught by Fukuzumi in figure 1.

The motivation for doing so would have been the cost efficient storage device as expressly taught by Fukuzumi in paragraphs 23 and 24.

Therefore, it would have been obvious to combine Fukuzumi with DeMargerie et al., Peng and Nakamura et al. to obtain the invention as specified in claims 19 and 22.

18. **Claim 20** discloses, "receiving synchronously third write data **["Seq#3", Figure 3, Nakamura et al.]** from the first primary subsystem at the intermediate storage system, the third write data being received at the intermediate subsystem after the first write data **["Seq#1", Figure 1, Nakamura et al.]**".

"Associating the third write data with third write order information; transmitting asynchronously the third write data **[Paragraph 80]** and the third write order information **["Seq#3", Figure 3, Nakamura et al.]** to the first secondary subsystem **["S-Vol" 111-1&2, Figure 1, Paragraph 34]**"

"Wherein the first and third write data have the same destination address **["S-Vol" 111-1, Figure 1, Paragraph 34]**, the destination address identifying a storage area in the first secondary subsystem"

"Wherein the first and third write order information is used to store the first write data to the identified storage area prior to storing the third write data to the identified storage area **["Write data are rearranged in the sequence number within the RCU 104", Paragraph 80]**"

19. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US 2002/0078296), De Margerie et al. (US 6,859,865), Fukuzumi (US

2002/0083263) and Peng (US 2002/0122601) as applied to claim 19 above, and further in view of Hakenberg et al. (US 2003/0198250).

20. As per **claim 21**, Nakamura et al., De Margerie et al., Fukuzumi and Peng disclose, "transmitting a request to prepare the first, second, and third write data for storage in the first and second secondary subsystems **[Transmitting data write acknowledgement after each write data (Inherent in synchronous mirroring), Column 4, Line 54, De Margerie et al.]**, the prepare request being transmitted to the first and second secondary subsystems from the intermediate subsystems".

"Transmitting a request to validate the write data that have been prepared according to the prepare request **[Transmitting data write acknowledgement (Inherent in synchronous mirroring), Column 4, Line 54, De Margerie et al.]**, the validate request being transmitted to the first and second secondary subsystem from the intermediate subsystem that identifies the write data to be prepared"

Nakamura et al., Fukuzumi, De Margerie et al. and Peng do not disclose expressly, "the prepare request including a reference sequence number".

Hakenberg et al. disclose sending an acknowledgement including sequence number to the transmitter in paragraph 40.

Nakamura et al., De Margerie et al., Fukuzumi, Peng and Hakenberg et al. are analogous art because they are from the same field of endeavor of data management.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Nakamura et al., De Margerie et al. and Peng by including sequence number to an acknowledgment as taught by Hakenberg et al. in paragraph 40.

The motivation for doing so would have been to detect bit errors in the compressed packet as expressly taught by Hakenberg et al. in paragraph 13.

Therefore, it would have been obvious to combine Hakenberg et al. with Nakamura et al., De Margerie et al., Fukuzumi and Peng for the benefit of error detection to obtain the invention as specified in claim 21.

21. Claims 6, 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US 2002/0078296), Fukuzumi (US 2002/0083263) and De Margerie et al. (US 6,859,865) as applied to claims 4 and 14 above, and further in view of Kaiya et al. (US 2003/0028737).

22. As per **claim 6**, Nakamura et al., Fukuzumi and De Margerie et al. disclose the remote copy system recited in claim 4.

Nakamura et al., Fukuzumi and De Margerie et al. do not disclose expressly, "first and second primary bitmaps provided at the first and second primary subsystems;

first and second intermediate bitmaps provided at the intermediate subsystem; and first and second secondary bitmaps provided at the first and second secondary subsystems, wherein the first and second primary bitmaps are associated with the first intermediate bitmap and the first and second secondary bitmaps are associated with the second intermediate bitmap, wherein the bitmaps are used during a resynchronization process to determine and copy only data have been changed since suspension of mirroring of a paired volumes."

Kaiya et al. disclose bitmaps provided at each subsystem, which indicates the copying condition of each area in Figure 1 and paragraph 42.

Nakamura et al., Fukuzumi, De Margerie et al. and Kaiya et al. are analogous art because they are from the same field of endeavor of controlling a plurality of storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Nakamura et al., Fukuzumi and De Margerie et al. by including bitmap in each subsystem as taught by Kaiya et al. in figure 1.

The motivation for doing so would have been to reduce the amount of memory occupied by the control information as expressly taught by Kaiya et al. in paragraph 43.

Therefore, it would have been obvious to combine Kaiya et al. with Nakamura et al., Fukuzumi and De Margerie et al. for the benefit of smaller memory occupation to obtain the invention as specified in claim 6.

23. As per **claim 16**, Nakamura et al., Fukuzumi and De Margerie et al. disclose the storage subsystem recited in claim 14.

Nakamura et al., Fukuzumi and De Margerie et al. do not disclose expressly, "first and second primary bitmaps provided at the first and second primary subsystems; first and second intermediate bitmaps provided at the intermediate subsystem; and first and second secondary bitmaps provided at the first and second secondary subsystems, wherein the first and second primary bitmaps are associated with the first intermediate bitmap and the first and second secondary bitmaps are associated with the second intermediate bitmap, wherein the bitmaps are used during a resynchronization process to determine and copy only data have been changed since suspension of mirroring of a paired volumes."

Kaiya et al. disclose bitmaps provided at each subsystem, which indicates the copying condition of each area in Figure 1 and paragraph 42.

Nakamura et al., Fukuzumi, De Margerie et al. and Kaiya et al. are analogous art because they are from the same field of endeavor of controlling a plurality of storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Nakamura et al., Fukuzumi and De Margerie et al. by including bitmap in each subsystem as taught by Kaiya et al. in figure 1.

The motivation for doing so would have been to reduce the amount of memory occupied by the control information as expressly taught by Kaiya et al. in paragraph 43.

Therefore, it would have been obvious to combine Kaiya et al. with Nakamura et al., Fukuzumi and De Margerie et al. for the benefit of smaller memory occupation to obtain the invention as specified in claim 16.

24. **Claim 17** discloses, "the first and second secondary volumes are configured to mirror the first and second primary volumes **[Figure 1, Nakamura et al., De Margerie et al.]**".

"The write data are received from the primary subsystems at the intermediate subsystem synchronously **["Synchronous Remote Mirroring", Column 4, Lines 53-54]**"

"The write data are transmitted to the secondary subsystem from the intermediate subsystem asynchronously **[Paragraph 80, Nakamura et al.]**"

Arguments Concerning Prior Art Rejections

1st Point of Argument

Regarding independent claim 1, the applicant argues that there is no motivation to combine DeMargerie with Nakamura. However, since the motivation to combine the two inventions is an extra layer of protection provided by DeMargerie as expressly taught in column 1, at lines 43-35, the combination is proper. Further, the examiner notes that such added layer of protection provided by cascaded mirroring is extremely common in the art.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

A. Claims No Longer in the Application

Claim 2 is cancelled.

B. Claims Rejected in the Application

Claims 1 and 3-23 have received a second action on the merits and are subject of a second action final.

C. Direction of Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.

If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

11/25/2007

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